COURSE PLAN - CAY 2019-20

Ref No:

## SRI KRISHNA INSTITUTE OF TECHNOLOGY BENGALURU



## COURSE PLAN

Academic Year 2019-20

Program:	B E – Electronics & Communication Engineering			
Semester :	5			
Course Code:	17EC53			
Course Title:	Electronic devices			
Credit / L-T-P:	4 / 4-0-0			
Total Contact Hours:	50			
Course Plan Author:	NARASIMHA MURTHY R			

Academic Evaluation and Monitoring Cell

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Note : Remove "Table of Content" before including in CP Book	
Each Course Plan shall be printed and made into a book with cover page	

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

## A. COURSE INFORMATION

#### 1. Course Overview

Degree:	BE	Program:	EC
Semester:	3	Academic Year:	2018
Course Title:	ELECTRONIC DEVICES	Course Code:	18EC33
Credit / L-T-P:	4 / 4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50 Hours	SEE Marks:	60 Marks
CIA Marks:	40 Marks	Assignment	1 / Module
Course Plan Author:	Dr. DEVANANDA S N	Sign	Dt:
Checked By:		Sign	Dt:
CO Targets	CIA Target :%	SEE Target:	%

**Note:** Define CIA and SEE % targets based on previous performance.

#### 2. Course Content

Content / Syllabus of the course as prescribed by University or designed by institute. Identify 2 concepts per module as in G.

Mod	Content	Teachi	Identified	Blooms
ule		ng	Module	Learning
		Hours	Concepts	Levels
1	Semiconductors: Bonding forces in solids, Energ	y 10	-Enenrgy bands	Understand
	bands, Metals, Semiconductors and Insulators, Direct and	k	- Intrinsic and	L2

COURSE	PLAN - 0	CAY	2019-20

-	Total	54	-	-
	Elements.			
	CMOS Process Integration, Integration of Other Circuit			
	Integrated Circuits: Background, Evolution of ICs.			
	metallization.		fundamentals	
	chemical vanour denosition photolithography Etching		– IC	
C	Diffusion Rapid Thermal Processing Ion implantation	10	techniques	I 2
E	Current-voltage Characteristics.	10	Eabrication	Understand
	Effects, Basic MOSEEI Operation- MOSEEI structure,			
	Capacitance - Voltage Characteristics and Frequency			
	terminal MOS structure- Energy band diagram, Ideal		characteristics	
	Equivalent Circuit and Frequency Limitations, MOSFETTwo		VI	L2
4	Field Effect Transistors: Basic pn JFET Operation,	10	–JFET operation	Understand
	narrowing, Avalanche breakdown.			
	cycle, specifications, Drift in the base region, Base			
	operation of a transistor, Cutoff, saturation, switching			
	coupled Diode model (Ebers–Moll Model), Switching		modes	
J	operation. Amplification with BITS, BIT Fabrication. The	10	- operating	L2
2	Binolar Junction Transistor Fundamentals of RIT	10	-BIT operation	Understand
	Junction, Solar Cells, Photodetectors. Light Emitting			
	Photodiodes: Current and Voltage in an Illuminated			
	avalanche breakdown, Rectifiers. Optoelectronic Devices		Applications	
	reverse bias, Reverse bias breakdown- Zener breakdown,		– Diode	
	Qualitative description of Current flow at a junction,		– Rectifiers	L2
2	P-N Junctions: Forward and Reverse biased junctions-	10	Diode biasing	Understand
	mobility, Hall Effect.			
	and Resistance, Effects of temperature and doping on			
	and Extrinsic materials. Conductivity and Mobility. Drift		semiconductors	
	Indirect semiconductors. Electrons and Holes. Intrinsic		Extrinsic	

## 3. Course Material

Books & other material as recommended by university (A, B) and additional resources used by course teacher (C).

1. Understanding: Concept simulation / video ; one per concept ; to understand the concepts ; 15 - 30 minutes

2. Design: Simulation and design tools used - software tools used ; Free / open source

3. Research: Recent developments on the concepts - publications in journals; conferences etc.

Modul	Details	Chapter	Availability
es		s in	
		book	
Α	Text books (Title, Authors, Edition, Publisher, Year.)	-	-
1, 2,	1. Ben. G. Streetman, Sanjay Kumar Banergee, "Solid State Electronic	3,5,7,8,	In Lib
3, 5	Devices", 7thEdition, Pearson Education, 2016, ISBN 978-93-325-	9	

	5508-2.		
4	2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and	9	In Lib
	Devices", 4th Edition, MCGraw Hill Education, 2012, ISBN 978-0-		
	07-107010-2.		
В	Reference books (Title, Authors, Edition, Publisher, Year.)	-	-
1, 2	1. S. M. Sze, Kwok K. Ng, "Physics of Semiconductor Devices", 3rd		In Lib
	Edition, Wiley, 2018.		
1, 2	2. A. Bar-Lev, "Semiconductor and Electronic Devices", 3rd Edition, PHI 1993		In Lib
C	Concent Videos or Simulation for Understanding		
	https://nptel.ac.in/courses/117101106/	_	
C2			
C3			
C4			
C5			
C6			
C7			
C8			
C9			
C10			
D	Software Tools for Design	-	-
E	Recent Developments for Research	-	-
	Others (Web, Video, Simulation, Notes etc.)		
<b>F</b>	Others (Web, Video, Simulation, Notes etc.) https://nptel.ac.in/courses/117101106/		

#### 4. Course Prerequisites

Refer to GL01. If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

Students mu	st have le	arnt the fo	ollowina (	Courses / T	Topics y	with a	described	Content .	
Students mu	St nuve ie	and the re	onowing (		i opics	wwitchi v	acscribea	content .	

Mod	Course	Course Name	Topic / Description	Sem	Remarks	Blooms
ules	Code					Level
1	_	_	Electronic Tubes / Knowledge of	_	Gap	Understa
			Tube Amplifier		A seminar on	nd L2
					Electron Tubes &	
					amplifiers	
3	15IT35	Electronics	Oscilloscopes / Knowledge of	3	-	Understa
		Instrumentatio	oscillators			nd L2
		n				
3	15EC36	Engineering	Steady Magnetic Fields/	3	_	Understa
		Electromagnet	Knowledge of fields			nd L2
		ics				
5	15MAT3	Mathematics-	Vector Integration / Knowledge	3	-	Understa
	1	111	of vector analysis			nd L2
-						
-						

#### 5. Content for Placement, Profession, HE and GATE

The content is not included in this course, but required to meet industry & profession requirements and help students for Placement, GATE, Higher Education, Entrepreneurship, etc. Identifying Area / Content requires experts consultation in the area.

Topics included are like, a. Advanced Topics, b. Recent Developments, c. Certificate Courses, d. Course Projects, e. New Software Tools, f. GATE Topics, g. NPTEL Videos, h. Swayam videos etc.

	-		-	
Mod	Topic / Description	Area	Remarks	Blooms
ules				Level
1	https://nptel.ac.in/courses/11710110	nptel		Understa
	<u>6/</u>			nd L2
3				
3				
5				
-				
-				

#### **B. OBE PARAMETERS**

#### 1. Course Outcomes

Expected learning outcomes of the course, which will be mapped to POs. Identify a max of 2 Concepts per Module. Write 1 CO per Concept.

Mod	Course	Course Outcome	Teach.	Concept	Instr	Assessm	Blooms'
ules	Code.#	At the end of the course,	Hours		Method	ent	Level

	COURSE PLAN – CAY 2019–20										
		student should be able to				Method					
1	18EC33.1	Understand the principles of	5	Energy	Lecture	Slip Test	Understand				
		semiconductor Physics		bands			L2				
1	18EC33.2	Understand the working	5	Electrons	Lecture/	Assignme	Understand				
		principles of semiconductor		and Holes,	Tutorial	nt	L2				
		devices.									
2	18EC33.3	Understand the principles and	5	Forward	Lecture	Assignme	Understand				
		characteristics of semiconductor		and		nt	L2				
		diodes.		Reverse							
				biased							
				junctions							
2	18EC33.4	Understand the applications of	5	applicatio	Lecture	Slip Test	Understand				
		semiconductor diodes.		ns of			L2				
				semicondu							
				ctor							
				diodes							
3	18EC33.5	Utilize the mathematical models	5	BJT	Lecture	Slip test	Understand				
		of bipolar junction transistors		operation			L2				
		for circuits and systems									
3	18EC33.6	Understand the operating	5	Amplificati	Lecture/	Assignme	Understand				
		principle of BJT.		on	Tutorial	nt	L2				
4	18EC33.7	Utilize the mathematical models	5	JFET	Lecture/	Assignme	Understand				
		of MOS transistors for circuits		Operation	Tutorial	nt	L2				
		and systems.									
4	18EC33.8	Understand the operating	5	MOSFET	Lecture/	Assignme	Understand				
		principle of MOS transistors.		Operation	Tutorial	nt	L2				
5	18EC33.9	Understand the fabrication	5	Fabricatio	Lecture	Assignme	Understand				
		process of semiconductor		n		nt	L2				
		devices .									
5	18EC33.10	Understand the CMOS IC	5	Integrated	Lecture	Assignme	Understand				
		technology.		Circuits		nt	L2				
-	-	Total	50	-	-	-	L2-L2				

## 2. Course Applications

Write 1 or 2 applications per CO.

Students should be able to employ / apply the course learnings to  $\ldots$ 

	· · · · · · · · · · · · · · · · · · ·		
Mod	Application Area	CO	Level
ules	Compiled from Module Applications.		
1	Analog circuit design is used for designing rectifiers, RPS.	CO1	L2
1	Analog circuit design is used for designing voltage regulators	CO2	L2
2	Analog circuit design is used for designing operational amplifiers.	CO3	L2
2	Analog circuit design is used for designing linear regulators.	CO4	L2
3	Analog circuit design is used for designing oscillators.	CO5	L2
3	Analog circuit design is used for designing active filters.	CO6	L2

	COURSE PLAN – CAY 2019–20		
4	Analog circuit design is used for designing phase locked loops.	C07	L2
4	Analog circuit design is used for designing oscillators.	CO8	L2
5	Analog circuit design is used for designing active filters.	CO9	L2
5	Analog circuit design is used for designing phase locked loops.	CO10	L2

## 3. Mapping And Justification

CO – PO Mapping with mapping Level along with justification for each CO–PO pair.

To attain competency required (as defined in POs) in a specified area and the knowledge & ability required to accomplish it.

Mod	Mod Mapping		Маррі	Justification for each CO-PO pair	Lev
ules			ng		el
			Level		
-	СО	РО	-	'Area': 'Competency' and 'Knowledge' for specified 'Accomplishment'	-
1	CO1	PO1	3	The basic engineering knowledge is applied for the basic analog circuit coding.	L2
1	CO1	PO2		Performing experiment allows the easy analysis of problems.	L2
1	CO1	PO3		Designing a analog system to meet the specific needs within the realistic constraints can be done.	L6
	CO2	PO1		The basic engineering knowledge is applied for the basic analog circuit coding.	
2	CO2	PO2		Performing experiment allows the easy analysis of problems.	
2	CO2	PO3		Designing a analog system to meet the specific needs within the realistic constraints can be done.	
2	CO3	PO1		The basic engineering knowledge is applied for the basic analog circuit coding.	
	CO3	PO2		Performing experiment allows the easy analysis of problems.	
	CO3	PO3		Designing a analog system to meet the specific needs within the realistic constraints can be done.	
	CO4	PO1		The basic engineering knowledge is applied for the basic analog circuit coding.	
	CO4	PO2		Performing experiment allows the easy analysis of problems.	
	CO4	PO3		Designing a analog system to meet the specific needs within the realistic constraints can be done.	
	CO5	PO1		The basic engineering knowledge is applied for the basic analog circuit coding.	
5	CO5	PO2		Performing experiment allows the easy analysis of problems.	
5	CO5	PO3		Designing a analog system to meet the specific needs within the realistic constraints can be done.	
5	CO6	PO1		The basic engineering knowledge is applied for the basic analog circuit coding.	
	CO6	PO2		Performing experiment allows the easy analysis of problems.	
	CO6	PO3		Designing a analog system to meet the specific needs within the realistic constraints can be done.	

COURSE PLAN – CAY 2019–20								
	C07	PO1	The basic engineering knowledge is applied for the basic analog					
			circuit coding.					
	C07	PO2	Performing experiment allows the easy analysis of problems.					
	C07	PO3	Designing a analog system to meet the specific needs within the					
			realistic constraints can be done.					
	CO8	PO1	The basic engineering knowledge is applied for the basic analog					
			circuit coding.					
	CO8	PO2	Performing experiment allows the easy analysis of problems.					
	CO8	PO3	Designing a analog system to meet the specific needs within the					
			realistic constraints can be done.					
	CO9	PO1	The basic engineering knowledge is applied for the basic analog					
			circuit coding.					
	CO9	PO2	Performing experiment allows the easy analysis of problems.					
	CO9	PO3	Designing a analog system to meet the specific needs within the					
			realistic constraints can be done.					
	CO10	PO1	The basic engineering knowledge is applied for the basic analog					
			circuit coding.					
	CO10	PO2	Performing experiment allows the easy analysis of problems.					
	CO10	PO3	Designing a analog system to meet the specific needs within the					
			realistic constraints can be done.					

## 4. Articulation Matrix

#### CO - PO Mapping with mapping level for each CO-PO pair, with course average attainment.

-	-	Course Outcomes	Program Outcomes					-										
Mod	CO.#	At the end of the course	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PO	PS	PS	PS	Lev
ules		student should be able to	1	2	3	4	5	6	7	8	9	10	11	12	01	02	03	el
1	18EC33.1	Understand the principles of semiconductor Physics	3	2	1													L2
1	18EC33.2	Understand the working principles of semiconductor devices.		2	1													L2
2	18EC33.3	Understand the principles and characteristics of semiconductor diodes.	3	2	1													L2
2	18EC33.4	Understand the applications of semiconductor diodes.	3	2	1													L2
3	18EC33.5	Utilize the mathematical models of bipolar junction transistors for circuits and systems	3	2	1													L2
3	18EC33.6	Understand the operating principle of BJT.	3	2	1													L2
4	18EC33.7	Utilize the mathematical	3	2	1													L2

		COURSE PLAN – CAY 2019–20							
		models of MOS transistors for							
		circuits and systems.							
4	18EC33.8	Understand the operating 3 2 1 L2							
		principle of MOS transistors.							
5	18EC33.9	Understand the fabrication 3 2 1 L2							
		process of semiconductor							
		devices .							
5	18EC33.1	Understand the CMOS IC 3 2 1 L2							
	0	technology.							
-	CS501PC	Average attainment (1, 2, 3 2 1 -							
		or 3)							
-	PO, PSO	1. Engineering Knowledge; 2. Problem Analysis; 3. Design / Development of Solutions; 4. Conduct							
		Investigations of Complex Problems; 5. Modern Tool Usage; 6. The Engineer and Society;							
		7. Environment and Sustainability; 8. Ethics; 9. Individual and Teamwork; 10. Communication;							
		11. Project Management and Finance; 12. Life-long Learning; S1. Software Engineering; S2. Data							
		Base Management; S3.Web Design							

## 5. Curricular Gap and Content

Topics & contents not covered (from A.4), but essential for the course to address POs and PSOs.

Mod	Gap Topic	Actions Planned	Schedule Planned	<b>Resources Person</b>	PO Mapping
ules					
1					
2					
3					
4					
5					

### 6. Content Beyond Syllabus

Topics & contents required (from A.5) not addressed, but help students for Placement, GATE, Higher Education, Entrepreneurship, etc.

Mod	Gap Topic	Area	Actions	Schedule	Resources	PO Mapping
ules			Planned	Planned	Person	
1						
1						
2						
2						
3						
3						
4						
4						
5						
5						

## C. COURSE ASSESSMENT

#### 1. Course Coverage

Assessment of learning outcomes for Internal and end semester evaluation. Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

Mod	Title	Teach		No. of	quest		CO	Levels		
ules			CIA-	CIA-	CIA-	Asg	Extra	SEE		
		Hours	1	2	3		Asg			
1	Semiconductors	10	2	-	-	1	1	2	CO1, CO2	L2
2	P–N Junctions	10	2	-	-	1	1	2	CO3, CO4	L2
3	Bipolar Junction Transistor	10	-	2	-	1	1	2	CO5, CO6	L2
4	Field Effect Transistors	10	-	2	-	1	1	2	CO7, C08	L2
5	Fabrication of p-n junctions	10	-	-	4	1	1	2	CO9,	L2
									CO10	
-	Total	50				5	5	10	-	-

#### 2. Continuous Internal Assessment (CIA)

Assessment of learning outcomes for Internal exams. Blooms Level in last column shall match with A.2.

Mod	Evaluation	Weightage in	CO	Levels
ules		Marks		
1, 2	CIA Exam - 1	30	CO1, CO2, CO3,Co4	L2,L2,L2,L2
3, 4	CIA Exam - 2	30	CO5, CO6, CO7, C08	L2,L2,L2,L2
5	CIA Exam - 3	30	CO9, CO10	L2,L2
1, 2	Assignment – 1	10	CO1, CO2, CO3,Co4	L2,L2,L2,L2
3, 4	Assignment – 2	10	CO5, CO6, CO7, C08	L2,L2,L2,L2
5	Assignment – 3	10	CO9, CO10	L2,L2
1, 2	Seminar – 1		-	-
3, 4	Seminar – 2		_	_
5	Seminar – 3		-	_
1, 2	Quiz – 1		_	_
3, 4	Quiz – 2		_	_
5	Quiz – 3		-	-
1 -	Other Activities – Mini Project	-	CO9, CO10	L2,L2
5				
	Final CIA Marks	40	-	-

# D1. TEACHING PLAN - 1

## Module – 1

Title:	Semiconductors	Appr	10 Hrs
		Time:	
а	Course Outcomes	CO	Bloom
			S
-	At the end of the topic the student should be able to	-	Level
1	Understand the principles of semiconductor Physics	CO1	L2
2	Understand the working principles of semiconductor devices.	CO2	L2
b	Course Schedule	_	-
Class No	Portion covered per hour	-	-
1	Bonding forces in solids	CO1	L2
2	Energy bands,	CO1	L2
3	Metals, Semiconductors and Insulators,	C01	L2
4	Direct and Indirect semiconductors,	CO1	L2
5	Electrons and Holes,	CO1	L2
6	Intrinsic and Extrinsic materials,	CO2	L2
7	Conductivity and Mobility,	CO2	L2
8	Drift and Resistance,	CO2	L2
9	Effects of temperature and doping on mobility,	CO2	L2
10	Hall Effect.	CO2	L2
С	Application Areas	-	-
-	Students should be able employ / apply the Module learnings to $\dots$	_	_
1	Analog circuit design is used for designing rectifiers, RPS.	CO1	L2
2	Analog circuit design is used for designing voltage regulators	CO2	L2
d	Review Questions	-	-
_	The attainment of the module learning assessed through following questions	-	_
1	Explain the Bonding forces in solids	CO1	L2
2	Explain the Energy bands,	CO1	L2
3	Explain the Metals, Semiconductors and Insulators,	CO1	L2
4	Explain the Direct and Indirect semiconductors,	CO2	L2
5	Explain theElectrons and Holes,	CO2	L2
6	Explain the Intrinsic and Extrinsic materials,	CO2	L2
7	Explain the Conductivity and Mobility,	CO2	L2
8	Explain the Drift and Resistance,	CO2	L2
9	Explain the Effects of temperature and doping on mobility,	CO2	L2
10	Explain the Hall Effect.	CO2	L2

е	Experiences	-	-
1		C01	L2
2			
3			
4		CO2	L2
5			

## Module - 2

Title:	P–N Junctions	Appr	7 Hrs
		Time:	
а	Course Outcomes	СО	Bloom
_	At the end of the topic the student should be able to	_	Level
1	Understand the principles and characteristics of semiconductor diodes.	CO3	L2
2	Understand the applications of semiconductor diodes.	CO4	L2
b	Course Schedule		
Class No	Portion covered per hour	-	-
11	Forward and Reverse biased junctions- Qualitative description of Current flow at a junction,	CO3	L2
12	Forward and Reverse biased junctions- Qualitative description of Current flow at a junction,	CO3	L2
13	reverse bias,	CO3	L2
14	Reverse bias breakdown- Zener breakdown,	CO3	L2
15	avalanche breakdown,	CO3	L2
16	Rectifiers.	CO4	L2
17	Optoelectronic Devices Photodiodes: Current and Voltage in an Illuminated Junction,	CO4	L2
18	Solar Cells, Photodetectors.	CO4	L2
19	Light Emitting Diode: Light Emitting materials.	CO4	L2
20	Light Emitting Diode: Light Emitting materials.	CO4	L2
C	Application Areas	-	-
_	Students should be able employ / apply the Module learnings to	_	-
1	Analog circuit design is used for designing voltage regulators	CO3	L2
2	Analog circuit design is used for designing operational amplifiers.	C04	L2
d	Review Questions		
-	The attainment of the module learning assessed through following questions	_	-
14	Explain the Forward biased junctions- Qualitative description of Current flow at a junction.	CO3	L2
15	Explain the Reverse biased junctions- Qualitative description of Current	CO3	L2

	flow at a junction.		
16	Explain the reverse biasing in semiconductor diode.	CO3	L2
17	Explain the Reverse bias breakdown and Zener breakdown,	CO4	L2
18	Explain the avalanche breakdown.	CO4	L2
19	Explain the Rectifiers. List the types of rectifiers.	CO4	L2
20	Explain the Optoelectronic Devices( Photodiodes).	CO4	L2
21	Explain the working and construction Solar Cells, Photodetectors.	CO4	L2
22	Explain the working and constructionLight Emitting Diode.	CO4	L2
е	Experiences	-	-
1		CO3	L2
2			
3			
4		CO4	L2
5			

#### COURSE PLAN - CAY 2019-20

## E1. CIA EXAM - 1

## a. Model Question Paper - 1

Crs		18EC33	Sem:	111	Marks:	30	Time:	90 minut	) minutes		
Coa	e:										
Cou	rse:	ELECTRON	IC DEVICES	)					1		
-	-	Note: Ans	e : Mark	СО	Level						
		1, 2						S			
1	a	Explain the	Bonding	forces in	solids			8	CO1	L2	
	b	Explain the	e Energy ba	ands,				8	CO1	L2	
	с	Explain the	e Metals, S	emicondu	ictors and In	sulators,		9	CO1	L2	
					OR						
2	a	Explain the	e Intrinsic a	and Extrir	nsic materials	5,		8	CO1	L2	
	b	Explain the	e Conducti	vity and M	/lobility,			8	CO1	L2	
	с	Explain the	e Drift and	Resistan	ce,			9	CO1	L2	
3	a	Explain th	e Reverse	biased	junctions-	Qualitati	ve description	of 8	CO3	L2	
		Current flo	w at a jun	ction.							
	b	Explain the	e reverse b	iasing in	semiconduct	or diode.		8	CO3	L2	
	с	Explain the	e Reverse b	oias break	down and Z	ener brea	akdown,	9	CO4	L2	
					OR						
4	a	Explain the	e avalanche	e breakdo	wn.			8	CO4	L2	
	b	Explain the	e Rectifiers	. List the	types of rect	ifiers.		8	CO4	L2	
	с	Explain the	e working a	and const	ructionLight	Emitting	Diode.	9			

#### b. Assignment -1

			Model A	Assignment Q	uestions				
Crs C	Code: 18EC	3 Sem:	III	Marks:	5	Time:	90 - 1	120 mi	nutes
Cour	se: Electr	onic devices			Module : 1	, 2			
Note	Each stude	nt to answer 2	–3 assig	nments. Each	assignment	carries	equal	mark.	
SNo	USN		Assign	iment Descr	iption		Mark	CO	Level
							S		
1	1KT18EC00	1 Explain the	Bonding	forces in solid	ds		5	C01	L2
2	1KT18EC00	3 Explain the	Energy b	ands,			5	CO1	L2
3	1KT18EC00	5 Explain the	Metals, S	emiconducto	rs and Insula	ators,	5	C01	L2
4	1KT18EC00	8 Explain the	Direct ar	nd Indirect ser	niconductor	s,	5	C01	L2
5	1KT18EC00	9 Explain theE	lectrons	and Holes,			5	CO1	L2
6	1KT18EC01	0 Explain the	Intrinsic	and Extrinsic	materials,		5	CO1	L2
7	1KT18EC01	1 Explain the	Conduct	ivity and Mob	ility,		5	C01	L2
8	1KT18EC01	2 Explain the	Drift and	Resistance,			5	CO1	L2
9	1KT18EC01	3 Explain the mobility,	Effects	of temperatu	ire and dop	oing on	5	CO1	L2
10	1KT18EC01	4 Explain the	Hall Effe	ct.			5	CO1	L2
11	1KT18EC01	5 Explain the description	Forward of Curre	d biased jur nt flow at a iu	ictions– Quanction.	alitative	5	CO2	L2
12	1KT18EC01	6 Explain the	Revers	e biased iun	ctions- Ou	alitative	5	CO2	L2
		description	of Curre	nt flow at a ju	nction.				
13	1KT18EC01	7 Explain the	reverse k	piasing in sem	iconductor	diode.	5	CO2	L2
14	1KT18EC01	8 Explain the breakdown,	Revers	e bias break	down and	Zener	5	CO2	L2
15	1KT18EC01	9 Explain the	avalanch	e breakdown.			5	CO2	L2
16	1KT18EC02	0 Explain the	Rectifier	s. List the type	es of rectifie	rs.	5	CO2	L2
17	1KT18EC02	1 Explain the	Opto-ele	ectronic Devic	es( Photodio	des).	5	CO2	L2
18	1KT17EC00	1 Explain the Photodetect	working	g and constr	uction Sola	r Cells,	5	CO2	L2
19	1KT16EC03	0 Explain the	working	and construc	tion Light E	Emitting	5	CO2	L2
		Diode.							
20	DIP	Explain the	Rectifier	s. List the type	es of rectifie	rs.	5	CO2	L2
21	DIP	Explain the	Optoelec	tronic Device	s( Photodioc	les).	5	CO2	L2
22	DIP	Explain the Photodetect	working ors.	g and constr	uction Sola	r Cells,	5	CO2	L2
23	DIP	Explain the Diode.	working	and construc	tion Light E	Emitting	5	CO2	L2

Note: A distinct assignment to be assigned to each student.

## D2. TEACHING PLAN – 2

#### Module – 3

Title: Bipolar Junction Transistor

		Time:	
а	Course Outcomes	СО	Bloom s
-	At the end of the topic the student should be able to	-	Level
1	Utilize the mathematical models of bipolar junction transistors for	CO5	L2
	circuits and systems		
2	Understand the operating principle of BJT.	CO6	L2
b	Course Schedule		
Class No	Portion covered per hour	-	-
21	Fundamentals of BJT operation,	CO5	L2
22	Amplification with BJTS,	CO5	L2
23	BJT Fabrication,	CO5	L2
24	The coupled Diode model (Ebers-Moll Model),	CO5	L2
25	The coupled Diode model (Ebers-Moll Model),	CO5	L2
26	Switching operation of a transistor,	CO6	L2
27	Cutoff, saturation, switching cycle,	CO6	L2
28	Cutoff, saturation, switching cycle,	CO6	L2
29	specifications, Drift in the base region,	CO6	L2
30	Base narrowing, Avalanche breakdown.	CO6	L2
С	Application Areas	-	-
-	Students should be able employ / apply the Module learnings to	-	-
1	Analog circuit design is used for designing operational amplifiers.	CO5	L2
2	Analog circuit design is used for designing linear regulators.	CO6	L2
d	Review Questions	-	-
-	The attainment of the module learning assessed through following	-	-
	questions		
18	Explain the working of BJT operation,	CO5	L2
19	Explain the working of bjt as an Amplifier.	CO5	L2
20	Explain the BJT Fabrication,	CO5	L2
21	Explain the The coupled Diode model (Ebers-Moll Model),	CO6	L2
22	Explain the Switching operation of a transistor,	CO6	L2
23	Explain the fallowing in terms of bjt - Cutoff, saturation, switching cycle,	CO6	L2
24	Explain the Base narrowing, Avalanche breakdown.	CO6	L2
е	Experiences		
1			
2			
3			
4		CO6	L2

5

## Module - 4

Title:	Field Effect Transistors	Appr	13 Hrs
		Time:	
а	Course Outcomes	СО	Bloom
			S
-	At the end of the topic the student should be able to	-	Level
1	Utilize the mathematical models of MOS transistors for circuits and systems.	C07	L2
2	Understand the operating principle of MOS transistors.	C08	L2
b	Course Schedule		
Class No	Portion covered per hour	-	-
31	Basic pn JFET Operation,	C07	L2
32	Equivalent Circuit	C07	L2
33	Frequency Limitations,	C07	L2
34	MOSFET Two terminal MOS structure- Energy band diagram,	C07	L2
35	MOSFET Two terminal MOS structure- Energy band diagram,	C07	L2
36	Ideal Capacitance - Voltage Characteristics and Frequency Effects,	C08	L2
37	Ideal Capacitance - Voltage Characteristics and Frequency Effects,	CO8	L2
38	Basic MOSFET Operation- MOSFET structure,	CO8	L2
39	Basic MOSFET Operation- MOSFET structure,	CO8	L2
40	Current-Voltage Characteristics.	CO8	L2
С	Application Areas	-	-
_	Students should be able employ / apply the Module learning to	-	-
1	Analog circuit design is used for designing active filters.	C07	L2
2	Analog circuit design is used for designing oscillators.	CO8	L2
d	Review Questions		-
-	The attainment of the module learning assessed through following questions	_	-
32	Explain theBasic pn JFET Operation,	C07	L2
33	Explain the the jfet Equivalent Circuit	C07	L2
34	Explain the Frequency Limitations of jfet	C07	L2
35	Explain the JFET Two terminal MOS structure with neat Energy band diagram.	C07	L2
36	Explain the Ideal Capacitance and Voltage Characteristics of IFET.	C07	L2
37	Explain the Basic MOSFET Operation- MOSFET structure.	C08	L2
38	Explain the Current–Voltage Characteristics of MOSFET.	C08	L2
39	Explain the Current-Voltage Characteristics of MOSFET.	C08	L2
40	Explain the Frequency Effects of JFET.	C08	L2

е	Experiences	_	-
1			
2			
3			
4			
5			

## E2. CIA EXAM – 2

## a. Model Question Paper - 2

Crs		18EC33	Sem:	III	Marks:	30	Time:	90 minut	minutes				
Cod	e:												
Cou	rse:	Electronic	devices						1				
-	-	Note: Ans	swer all o	question	s, each carr	y equal I	marks. Modu	le : Mark	CO	Level			
		3, 4						S					
1	a	Explain the	e qualitati	ve descrip	otion of curre	nt flow at	a junction.	8	CO5	L2			
	b	Explain the	e Reverse	bias brea	kdown in a PN	l junction		8	CO6	L2			
		Explain the	e differend	e betwee	n Zener breal	kdown an	d Avalanche	•	606				
	С	breakdowr	ı.					9	C06	L2			
		OR											
2	_	Explain the	e Piece –W	'ise linear	approximatio	on of junc	tion Diode	0	COG	1.2			
2	a	characteris	stics.					0					
	b	Explain the	e Optical g	generatio	n of carrier in	a PN junc	tion.	8	CO6	L2			
	С	Explain the	e configur	ation of a	Solar cell.			9	CO5	L2			
3	a	With schen	natic expl	ain P-I-N	Photo diode.			8	C07	L2			
	b	Explain the	e effect of	Injection	Electrolumin	iscence.		8	C07	L2			
	с	Explain dif	ferent typ	es of ligh	t emitting ma	terials.		9	CO8	L2			
		OR											
4	a	Explain the	e external	contral o	f current in re	everse bia	sed PN junctio	on. 8	CO8	L2			
	b	With schen	natic expl	ain P-N-F	rtransistorwit	h biased:	condition.	8	C07	L2			
	с	Explain the	e Amplific	ation in a	common em	itter trans	istor circuit.	9	CO8	L2			

## b. Assignment - 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions										
Crs C	ode:	18EC33	Sem:	III	Marks:	5	Time:	90 - 120 minutes		tes
Cours	se: I	ELECTRO	NIC DEVICES		4	Modu	le : 3, 4			
Note:	Note: Each student to answer 2–3 assignments. Each assignment carries equal mark.									
SNo	U	ISN		Assign	ment Des	criptio	on	Mark	СО	Level
								S		
1 1KT18EC001 Explain the working of BJT operation,						CO5	L2	L2		
2 1KT18EC003 Explain the working of bjt as an Amplifier.				CO5	L2	L2				

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		COURSE PLAN – CAY 2019–20			
3	1 KT1 8EC005	Explain the BJT Fabrication,	CO5	L2	L2
4	1 KT1 8EC008	Explain the The coupled Diode model (Ebers-Moll Model),	CO6	L2	L2
5	1KT18EC009	Explain the Switching operation of a transistor,	CO6	L2	L2
6	1KT18EC010	Explain the fallowing in terms of bjt – Cutoff, saturation,	CO6	L2	L2
		switching cycle,			
7	1KT18EC011	Explain the Base narrowing, Avalanche breakdown.	CO6	L2	L2
8	1KT18EC012	Explain theBasic pn JFET Operation,	C07	L2	L2
9	1KT18EC013	Explain the the jfet Equivalent Circuit	C07	L2	L2
10	1KT18EC014	Explain the Frequency Limitations of jfet	C07	L2	L2
11	1KT18EC015	Explain the JFET Two terminal MOS structure with neat	C07	L2	L2
		Energy band diagram,			
12	1KT18EC016	Explain the Ideal Capacitance and Voltage Characteristics	C07	L2	L2
		of JFET.			
13	1KT18EC017	Explain the Basic MOSFET Operation- MOSFET structure,	CO8	L2	L2
14	1KT18EC018	Explain the Current-Voltage Characteristics of MOSFET.	CO8	L2	L2
15	1KT18EC019	Explain the Current-Voltage Characteristics of MOSFET.	CO8	L2	L2
16	1KT18EC020	Explain the Frequency Effects of JFET.	CO8	L2	L2
17	1KT18EC021	Explain the working of BJT operation,	CO5	L2	L2
18	1KT17EC001	Explain the working of bjt as an Amplifier.	CO5	L2	L2
19	1KT16EC030	Explain the BJT Fabrication,	CO5	L2	L2
20	DIP	Explain the The coupled Diode model (Ebers-Moll Model),	CO6	L2	L2
21	DIP	Explain the Switching operation of a transistor,	CO6	L2	L2
22	DIP	Explain the fallowing in terms of bjt - Cutoff, saturation,	CO6	L2	L2
		switching cycle,			
23	DIP	Explain the working of BJT operation,	CO5	L2	L2

# D3. TEACHING PLAN – 3

## Module - 5

Title:	Fabrication of p-n junctions and Integrated Circuits	Appr	10 Hrs
		Time:	
а	Course Outcomes	СО	Bloom
			S
-	At the end of the topic the student should be able to	-	Level
1	Understand the fabrication process of semiconductor devices .	CO9	L2
2	Understand the CMOS IC technology.	CO10	L2
b	Course Schedule	-	-
Class	Portion covered per hour	-	-
No			
41	Thermal Oxidation,	CO9	L2

42	Diffusion,	CO9	L2
43	lon implantation,	CO9	L2
44	Rapid Thermal Processing,	CO9	L2
45	chemical vapour deposition,	CO9	L2
46	Background, Evolution of ICs,	CO10	L2
47	CMOS Process Integration,	CO10	L2
48	Integration of Other Circuit Elements.	CO10	L2
49	photolithography,	CO10	L2
50	Etching, metallization.	CO10	L2
С	Application Areas	-	-
-	Students should be able employ / apply the Module learnings to	-	-
1	Analog circuit design is used for designing oscillators.	CO9	L2
2	Analog circuit design is used for designing active filters.	CO10	L2
	Analog circuit design is used for designing phase locked loops.		
d	Review Questions	-	-
-	The attainment of the module learning assessed through following	-	-
	questions		
42	Explain the Thermal Oxidation method of fabrication.	CO9	L2
43	Explain the Diffusion fabrication.	CO9	L2
44	Explain the Ion implantation fabrication,	CO9	L2
45	Explain the Rapid Thermal Processing fabrication,	CO9	L2
46	Explain the chemical vapour deposition fabrication,	CO9	L2
47	Explain the Background and Evolution of ICs,	CO10	L2
48	Explain the CMOS Process Integration,	CO10	L2
49	Explain the Integration of Other Circuit Elements.	CO10	L2
50	Explain the photolithography,	CO10	L2
51	Explain the Etching, metallization.	CO10	L2
е	Experiences	-	-
1		CO10	L2
2		CO9	
3			
4		CO9	L2
5			

# E3. CIA EXAM - 3

## a. Model Question Paper - 3

Crs		18EC33	Sem:	111	Marks:	30	Time:	90 minutes		
Code:										
Course: Electronic devices										
-	-	Note: Ans	wer all qu	estions, e	ach carry	equal mai	ks. Modul	e : Mark	СО	Level
		5						S		

		COURSE PLAN – CAY 2019–20			
1	a	Explain the Thermal Oxidation method of fabrication.	8	CO9	L2
	b	Explain the Diffusion fabrication.	8	CO9	L2
	с	Explain the Ion implantation fabrication,	9	CO9	L2
		OR			
1	a	Explain the Rapid Thermal Processing fabrication,	8	CO9	L2
	b	Explain the chemical vapour deposition fabrication,	8	CO9	L2
	с	Explain the Background and Evolution of ICs,	9	CO9	L2
2	a	Explain the CMOS Process Integration,	8	CO10	L2
	b	Explain the Integration of Other Circuit Elements.	8	CO10	L2
	с	Explain the photolithography,	9	CO10	L2
		OR			
2	a	Explain the Integration of Circuit Elements.	8	CO10	L2
	b	Explain the photolithography,	8	CO10	L2
	с	Explain the Etching, metallization.	9	CO10	L2

# b. Assignment - 3

#### Note: A distinct assignment to be assigned to each student.

Model Assignment Questions										
Crs C	Code:	18EC33	Sem:	III	Marks:	5	Time:	90 - 120	) minut	es
Cour	se:	Electron	ic devices	1	1	Module :	5			
Note	: Each	student	to answer 2	-3 assignm	ents. Each	assignmer	nt carries equ	ial mark.		
SNo	ι ι	JSN		Assign	ment De	scription		Mark	CO	Level
								S		
1	1 IKT18EC001 Explain the Thermal Oxidation method of fabrication.						prication.	5	CO10	L2
2	1KT1	8EC003	Explain the	Diffusion fa	abrication			5	CO10	L2
3	1KT1	8EC005	Explain the Ion implantation fabrication,						CO9	L2
4	1KT1	8EC008	Explain the	plain the Rapid Thermal Processing fabrication,					CO9	L2
5	1KT1	8EC009	Explain the	plain the chemical vapour deposition fabrication,					CO9	L2
6	1KT1	8EC010	Explain the	Background	d and Evo	lution of IC	s,	5	CO9	L2
7	1KT1	8EC011	Explain the O	CMOS Proce	ess Integra	tion,		5	CO9	L2
8	1KT1	8EC012	Explain the I	ntegration	of Other O	Circuit Elemo	ents.	5	CO9	L2
9	1KT1	8EC013	Explain the p	photolithog	raphy,			5	CO9	L2
10	1KT1	8EC014	Explain the	Etching, m	etallizatio	າ.		5	CO9	L2
11	1KT1	8EC015	Explain the T	Thermal Ox	idation m	ethod of fal	prication.	5	CO9	L2
12	1KT1	8EC016	Explain the	Diffusion fa	abrication	1		5	CO9	L2
13	1KT1	8EC017	C017 Explain the Ion implantation fabrication,						CO10	L2
14	1KT1	8EC018	Explain the	plain the Rapid Thermal Processing fabrication, 5 CO10 L2						L2
15	1KT1	8EC019	Explain the	chemical va	apour dep	osition fabr	ication,	5	CO10	L2

	COURSE PLAN – CAY 2019–20										
16	51KT18EC020Explain the Background and Evolution of ICs,5CO10L2										
17	1KT18EC021	Explain the CMOS Process Integration,	5	CO10	L2						
18	1KT17EC001	Explain the Integration of Other Circuit Elements.	5	CO10	L2						
19	1KT16EC030	Explain the photolithography,	5	CO10	L2						
20	DIP	Explain the Etching, metallization.	5	CO10	L2						
21	DIP	Explain the Background and Evolution of ICs,	5	CO10	L2						
22	DIP	Explain the CMOS Process Integration,	5	CO10	L2						
23	DIP	Explain the Integration of Other Circuit Elements.	5	CO10	L2						

# F. EXAM PREPARATION

### 1. University Model Question Paper

Course:		Electronic c	levices				Month	/ Year	May /	2018
Crs C	ode:	18EC33	Sem:	111	Marks:	80	Time:		180 m	inutes
Mod	Not	Answer all	FIVE full ques	stions. Al	l questions carry	equal marks	i.	Marks	CO	Level
ule	е									

### 2. SEE Important Questions

Course:		Electronic dev	ectronic devices							2018
Crs C	ode:	18EC33	Sem:	7	Marks:	80	Time:		1 80 minutes	
	Not e	Answer all FIV	E full questio	ons. All ques	tions carry e	qual marks.	1	-	_	
Mod ule	Qno.	Important Que	estion					Mark s	СО	Year

# G. Content to Course Outcomes

#### 1. TLPA Parameters

#### Table 1: TLPA – Example Course

Мо	Course Content or Syllabus	Content	Blooms'	Final	Identifie	Instructi	Assessmen
dul	(Split module content into 2 parts which	Teachin	Learnin	Bloo	d Action	on	t Methods
e-	have similar concepts)	g Hours	g Levels	ms'	Verbs	Methods	to Measure
#			for	Level	for	for	Learning
			Content		Learning	Learning	
A	В	С	D	E	F	G	Н
1		3	– L1	L2	-	-	– Slip Test
			– L2		-	Lecture	-
						_	-
						_	
1		9	– L2	L2	_	-	-
			– L2		_	Lecture	Assignmen
						_	t
						Tutorial	_
						_	_
2		4	– L2	L2	_	_	_
			- L2		_	Lecture	Assianmen
						_	t
							_
2		2	-12	12		_	- Slin Test
						Locturo	Sub Lest
			- LZ		-	Lecture	_
						-	

	COURSE PLA	AN - CAY 2	2019-20				
3		5	– L1	L2	-	-	– Slip Test
			– L2		-	Lecture	-
						_	
3		12	– L2	L2	-	_	-
			– L2		_	Lecture	Assignmen
						_	t
						Tutorial	-
						_	-
4		8	– L2	L2	-	_	-
			– L1		_	Lecture	Assignmen
						_	t
						Tutorial	-
						_	-
4		8	– L2	L2	_	-	_
			– L2		_	Lecture	Assignmen
						_	t
						Tutorial	_
						_	_
5		5	– L2	L2	_	_	_
			– L2		_	Lecture	Assignmen
						_	t
						_	_
							_
5		5	– L2	L2	_	_	_
			– L2		_	Lecture	Assignmen
						_	t
						_	_
							_
		1		1			1

## 2. Concepts and Outcomes:

#### Table 2: Concept to Outcome - Example Course

Мо	Learning or	Identified	Final	Concept	CO Components	Course Outcome
dul	Outcome	Concepts	Concept	Justification	(1.Action Verb,	
e-	from study	from		(What all Learning	2.Knowledge,	
#	of the	Content		Happened from	3.Condition /	Student Should
	Content or			the study of	Methodology,	be able to
	Syllabus			Content / Syllabus.	4.Benchmark)	
				A short word for		
				learning or		
				outcome)		
A	Ι	J	K	L	М	N
1	-	-	Klystron	Comprehend the	- Understand	Understand the
	-	-	oscillator	working of	– Klystron	working of Klystron
				Klystron oscillator	Oscillator	Oscillator.

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					_	
1	_	_	Microwave	Examine the	– Analyze	Analyze the
.	_	_	transmission	transmission lines	- Transmission	transmission lines
			lines	using graphical	lines	using Graphical
				methods	– Graphical	methods.
					Methods	
					_	
2	_	_	Multiport	Implement the Z. Y	– Analyze	Analyze the Z. Y
	_	_	networks	and S parameters	– Multiport	and S parameters
				to Multiport	Networks	for a Multiport
				networks		network.
2	_	_	Microwave	Understand the	– Understand	Understand the
	_	_	passive	working of	– Microwave	working of
			devices	microwave passive	Passive Devices	different
				devices		microwave passive
						devices.
3	_	_	Striplines	Have knowledge of	- Understand	Understand micro,
	_	_		micro, parallel and	– Types of Stripline	parallel and
				shielded striplines		shielded striplines.
3	_	_	Antenna	Compute the	– Apply	Describe antenna
	_	_	parameters	antenna design	– Design	working using the
				characteristics	Characteristics	given parameters.
				using the	_	
				parameters	_	
4	_	_	Array of	Extend the	– Apply	Describe the
	_	_	point	antenna	- Array of Point	working of point
			sources	parameters to the	Sources	sources.
				array of point		
				sources		
4	_	-	Electric	Examine the field	- Analyze	Analyze the
	-	-	dipole	parameters of	– Electric Dipole	working of electric
			antennas	electric dipole	Antenna	dipole antenna.
				antennas		
5	_	_	Loop and	Explain the	- Understand	Explain the
	_	_	horn	working of horn	- Horn and Loop	working of horn
			antennas	and loop antennas	Antenna	and loop antennas.
5			Helical,	Compare the	- Understand	Compare the
			Parabola,	working of helical,	– Helical, Parabola,	working of helical,
			Yagi-Uda	parabola, Yagi–	Yagi-Uda and Log-	and Yagi-Uda
			and Log-	Uda and log-	periodic Antennas	antennas
			periodic	periodic antennas		
			antennas			